Amendments to the Specification

Please replace paragraphs **[0056]** - **[0057]** with the following rewritten paragraphs:

[0056] ~~Figs. 6(1)-6(5)~~Figs. 6(A)-6(E) are first schematics including sectional views showing steps of manufacturing the electro-optical device step by step;

[0057] ~~Figs. 7(b)-7(a)~~Figs. 7(A)-7(D) are second schematics including sectional views showing steps of manufacturing the electro-optical device step by step;

Please replace paragraph **[0123]** with the following rewritten paragraph:

[0123] As shown in ~~(Fig. 6(1),~~Fig. 6(A), the TFT array substrate 10 containing quartz, hard glass, or silicon is prepared. The TFT array substrate 10 is then pretreated. For example, the TFT array substrate 10 is preferably annealed at a high temperature ranging from about 900 to 1,300°C in an inert gas atmosphere preferably, such as nitrogen (N_2), so as to decrease deformation of the TFT array substrate 10 caused in subsequent steps at a high temperature.

Please replace paragraph **[0126]** with the following rewritten paragraph:

[0126] Next, as shown in ~~Fig. 6(2),~~Fig. 6(B), the semiconductor layers 1a included in the TFTs 30 are thermally oxidized at a temperature of about 900 to 1,300°C, preferably about 1,000°C, thereby forming lower gate-insulating sub-layers. Upper gate-insulating sub-layers may be subsequently each formed on the corresponding lower gate-insulating sub-layers by a vacuum CVD process or the like, if necessary. Thereby, insulating layers 2 that have a single- or multi-layer structure and contain high temperature oxide (HTO) and/or silicon nitride are formed (the insulating layers 2 include the above gate-insulating sub-layers). As a result, the semiconductor layers 1a have a thickness of about 30 to 150 nm and preferably 35 to 50 nm. The insulating layers 2 have a thickness of about 20 to 150 nm and preferably 30 to 100 nm.

Please replace paragraph **[0129]** with the following rewritten paragraph:

[0129] As shown in ~~Fig. 6(3),~~Fig. 6(C), a polysilicon layer is deposited over the base insulating layer 12 by a vacuum CVD process or the like, and phosphorus (P) is

thermally diffused in the polysilicon layer, thereby rendering the polysilicon layer conductive. Alternatively, P ions may be introduced into the polysilicon layer during the formation thereof instead of the thermal diffusion, thereby forming a doped polysilicon layer. The polysilicon layer preferably has a thickness of about 100 to 500 nm and preferably about 350 nm. The resulting polysilicon layer is then subjected to photolithography and etching, thereby forming the gate electrodes 3a, arranged in a predetermined pattern, including gate electrode portions for the TFTs 30. According to the manufacturing process of the invention, when the gate electrodes 3a are formed, the side walls 3b extending from the gate electrodes 3a are simultaneously formed. The side walls 3b are formed by depositing the polysilicon layer in the slots 12cv. In this case, since the bottoms of the slots 12cv are in contact with the corresponding scanning lines 11a, the side walls 3b are each electrically connected to the corresponding scanning lines 11a. Furthermore, according to the manufacturing process, the lower junction electrodes 719 are also formed during the formation of the gate electrodes 3a. Thereby, the lower junction electrodes 719 are arranged in a two-dimensional pattern shown in Fig. 2.

Please replace paragraph **[0134]** with the following rewritten paragraph:

[0134] Next, as shown in (~~Fig. 6(4),~~Fig. 6(D), the first interlayer insulating layer 41 is formed over the gate electrodes 3a by an atmospheric or vacuum CVD process using TEOS gas, TEB gas, or TMOP gas or the like. The first interlayer insulating layer 41 contains silicate glass, such as NSG, PSG, BSG, or BPSG; silicon nitride; or silicon dioxide and has a thickness of about 500 to 2,000 nm. The first interlayer insulating layer 41 is preferably annealed at a high temperature, for example, about 800°C, thereby enhancing properties thereof.

Please replace paragraph **[0136]** with the following rewritten paragraph:

[0136] As shown in ~~Fig. 6(5),~~Fig. 6(E), a second precursor film for the lower electrodes 71 having a thickness of about 100 to 500 nm and a predetermined pattern is formed on the first interlayer insulating layer 41 by sputtering Pt or the like. In this case, the second precursor film is formed such that the second contact holes 83 and third contact holes 881 are filled with such metal film. Thereby, the lower electrodes 71 are each electrically

connected to the corresponding heavily doped drain regions 1e and lower junction electrodes 719. The second precursor film is then etched, thereby forming the lower electrodes 71.

Please replace paragraphs **[0138]** - **[0139]** with the following rewritten paragraphs:

[0138] As shown in ~~Fig. 7(6),~~Fig. 7(A), the silicon dioxide sub-layer 75a is not etched but the third precursor film for the silicon nitride sub-layers 75b is etched such that the silicon nitride sub-layers 75b have a size slightly larger than that of the lower electrodes 71 of the pixel potential capacitor electrodes. Furthermore, the fourth precursor film for the capacitor electrodes 300 is then etched such that the capacitor electrodes 300 have substantially the same size as that of the lower electrodes 71. In such a configuration, based on the formation of the capacitor electrodes 300, the portions each disposed between the corresponding capacitor electrodes 300 and lower electrodes 71 substantially correspond to the dielectric layers 75 (see Fig. 4).

[0139] Alternatively, in ~~Fig. 7(6),~~Fig. 7(A), the third precursor film to form the silicon nitride sub-layers 75b and the fourth precursor film to form the capacitor electrodes 300 may be etched in one step to form the dielectric layers 75 and capacitor electrodes 300, and to thereby obtain the storage capacitors 70.

Please replace paragraphs **[0142]** - **[0144]** with the following rewritten paragraphs:

[0142] As shown in ~~Fig. 7(7),~~Fig. 7(B), the second interlayer insulating layer 42 is formed by an atmospheric or vacuum CVD process, preferably by a plasma CVD process, using, for example, TEOS gas or the like. The second interlayer insulating layer 42 contains silicate glass, such as NSG, PSG, BSG, or BPSG; silicon nitride; or silicon dioxide. When the capacitor electrodes 300 contain aluminum, the second interlayer insulating layer 42 must be formed at a low temperature by a plasma CVD process. The second interlayer insulating layer 42 has a thickness of about 500 to 1,500 nm. Then, the first contact holes 81, seventh contact holes 801, and fourth contact holes 882 are formed in the second interlayer insulating layer 42 by a dry etching process, such as a reactive ion etching process or a reactive ion beam etching process. In this case, the first contact holes 81 each extend to the corresponding heavily doped source regions 1d of the semiconductor layers 1a, the seventh contact holes 801 each extend to the corresponding capacitor electrodes 300, and the fourth contact holes 882 each extend to the corresponding lower junction electrodes 719.

[0143] As shown in ~~Fig. 7(8),~~Fig. 7(C), a fifth precursor film is formed on the entire surface of the second interlayer insulating layer 42 by a sputtering process or the like. The fifth precursor film contains light-shielding and low resistant metal, such as aluminum, metal silicide or the like and has a thickness of about 100 to 500 nm, preferably about 300 nm. The fifth precursor film is subjected to photolithography and etching to form the data lines 6a having a predetermined pattern. In this etching step, the first junction electrodes 6a1 and second junction electrodes 6a2 are also simultaneously formed. The first junction electrodes 6a1 each cover the corresponding seventh contact holes 801, and the second junction electrodes 6a2 each cover the corresponding fourth contact holes 882. A titanium nitride film is then formed over these components by a plasma CVD process or the like, and is etched such that the titanium nitride film remains only on the data lines 6a (see reference numeral 41TN shown in ~~Fig. 7(8)).~~Fig. 7(C)). However, the titanium nitride film may remain on the corresponding first junction electrodes 6a1 and second junction electrodes 6a2 and the titanium nitride film may remain over the entire surface of the TFT array substrate 10. The titanium nitride film and the fifth precursor film containing aluminum may be formed simultaneously, and subjected to etching in one step. (In this case, an obtained configuration is somehow different from that shown in Fig. 4.)

[0144] As shown in ~~Fig. 7(9),~~Fig. 7(D), the third interlayer insulating layer 43 is formed to cover the data lines 6a and the like by an atmospheric or vacuum CVD process using, for example, TEOS gas or the like, preferably by a plasma CVD process which allows film formation at a low temperature. The third interlayer insulating layer 43 contains silicate glass, such as NSG, PSG, BSG, or BPSG, silicon nitride, silicon dioxide or the like, and has a thickness of about 500 to 1,500 nm. The ninth contact holes 803 and sixth contact holes 804 are formed in the third interlayer insulating layer 43 by a dry etching process, such as a reactive ion etching process or a reactive ion beam etching process. The ninth contact holes 803 are formed to lead to the corresponding first junction electrodes 6a1, and the sixth contact holes 804 are formed to lead to the corresponding second junction electrodes 6a2.